In the outstanding Office Action, Claims 1 and 9 were objected to; Claims 1-3 and 5-9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al in view of Deleonibus; Claim 4 is rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al in view of Deleonibus and Misra et al; and Claim 10 was rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al in view of Deleonibus and Gardner et al.

Regarding the objection to Claims 1 and 9, these claims have been amended in light of the comments noted in the outstanding Office Action and as shown in the marked-up copy. Accordingly, it is respectfully requested this objection be withdrawn.

Claims 1-3 and 5-9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al in view of Deleonibus. This rejection is respectfully traversed.

Amended Claim 1 is directed to a method for fabricating an electronic component with a self-aligned source, drain and gate. The method includes forming a dummy gate on a silicon substrate, forming a source and a drain on either side of a channel, superficial, self-aligned siliciding of the source and drain, depositing at least one contact metal layer having a total thickness greater than a height of the dummy gate, polishing the at least one contact metal layer stopping at the dummy gate, and realizing a surface insulation. The method also includes replacing the dummy gate by at least one final gate separated from the substrate by a gate insulating layer and electrically insulating the source and drain.

The feature in which the method introduces in step (d) (the realization of a surface insulation) is described in the specification at least at page 6, lines 17-20, at page 12, lines 11-25, and at page 14, lines 30-33. The surface insulation can be conducted by a superficially oxidation of the contact metal layer (see dependent Claim 6), or by depositing a layer of dielectric material (see new Claim 11). The surface insulation is used as a stopping layer during planarization and as a protecting layer of the source and the drain regions.

When the planarization of the final gate is performed, the source and drain regions will be attacked. In addition, the material of the final grid can short-circuit the source and the drain.

Boyd does not teach or suggest a step of realizing a surface insulation after forming a dummy gate and before replacing the dummy gate by a final gate. The surface insulation of Boyd (reference 26 in Figure 1E and reference 62 in Figure 2F) is only a gate oxide layer. In the present invention, the gate oxide layer is reference 114 or 148.

Further, Deleonibus also does not disclose the realization of a surface insulation after forming a dummy gate and before replacing the dummy gate by a final gate. Accordingly, Applicants submit there is no motivation to one of ordinary skill in the art at the time the invention was made to realize a surface insulation after the steps of forming a dummy gate and of depositing contact layers and before the step of replacing the dummy gate by a final gate to prevent short-circuiting of the source and drain with the material of the final gate and to realize a stopping layer.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Further, regarding the additional rejections noted in the outstanding Office Action, it is respectfully noted each of these reject dependent claims and the additional publications of Misra et al and Gardner et al also do not teach or suggest the features recited in amended Claim 1. Accordingly, it is respectfully requested these rejections also be withdrawn.

In addition, a new Abstract has been added to correspond with U.S. standard patent practice. It is believed no new matter has been added.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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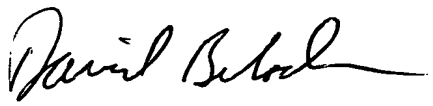

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IN THE CLAIMS

--1. (Amended) [Method] A method for fabricating an electronic component with a self-aligned source, drain and gate, comprising the [following] steps of:

a) [the formation of] forming a dummy gate [(112)] on a silicon substrate [(100)], said dummy gate defining a position for a channel [(121)] of the component[,];

b) at least one implantation of doping impurities in the substrate, to form a source [(118)] and a drain [(120)] on either side of the channel, using the dummy gate as an implanting mask[,];

c) superficial, self-aligned siliciding of the source and drain[,];

d) depositing at least one contact metal layer [of so-called contact metal (130), 132)] having a total thickness greater than [the] a height of the dummy gate, [and] polishing the at least one contact metal layer stopping at the dummy gate, and realizing a surface insulation; and

e) replacing the dummy gate by at least one final gate [(150, 160, 164)] separated from the substrate by a gate insulating layer [(148)], and electrically insulated from the source and drain.

2. (Amended) The method [Method] according to claim 1, [in which] wherein step d) comprises [the] depositing [of] a first metal layer [(130)] and, above the first metal layer, a second metal layer [(132)] having a greater mechanical resistance to polishing than the first

metal layer, [the] a thickness of the first metal layer being less than the height of the dummy gate, [but the] and a total thickness of the first and second metal layers being greater than the height of the dummy gate.

3. (Amended) [Method] The method according to claim 1, [also] further comprising, before siliciding, [the formation of] forming side spacers [(114, 116)] on [the] sides of the dummy gate.

4. (Amended) [Method] The method according to claim 3, [in which] wherein dual-layer spacers are formed comprising an attachment layer [(114)] in silicon oxide, in contact with the dummy gate, and a superficial layer [(116)] in silicon nitride.

5. (Amended) [Method] The method according to claim 2, [in which] wherein a metal of the first metal layer is chosen from among tungsten and titanium, and [in which] a metal of the second metal layer is chosen from among TaN, Ta and TiN.

6. (Amended) [Method] The method according to claim 1 [comprising, after polishing, superficial oxidation of], wherein the surface insulation comprises superficially oxidizing the at least one contact metal layer [or layers].

7. (Amended) [Method] The method according to claim 1, [in which] wherein the silicon substrate comprises a solid substrate[is used].

8. (Amended) [Method] The method according to claim 1, [in which] wherein the silicon substrate comprises a [substrate of] silicon on insulator substrate [type is used].

9. (Amended) [Method] The method according to claim 1, [in which] wherein step e) comprises [the removal of] removing the dummy gate, [formation of] forming the gate insulating layer [(148)], depositing at least one metal layer [(150, 160, 162), so-called] to form the final gate [layer], having an overall thickness equal to or greater than the height of the removed dummy gate[, and forming said metal layer].

10. (Amended) [Method] The method according to claim 9, further comprising, after [the formation of] forming the gate insulating layer [(148)], [the depositing of] depositing a first gate metal layer [(160)], [the depositing of] depositing at least one inter-gate dielectric layer [(162)], and [the] depositing [of] a second gate metal layer [(164)].

11. (New).--

IN THE ABSTRACT

Page 20 (New).

--ABSTRACT OF THE DISCLOSURE

A method for fabricating an electronic component with a self-aligned source, drain and gate. The method includes forming a dummy gate on a silicon substrate, in which the dummy gate defines a position for a channel of the component. The method also includes at least one implantation of doping impurities in the substrate, to form a source and a drain on either side of the channel, using the dummy gate as an implanting mask, superficial, self-aligned siliciding of the source and drain, depositing at least one contact metal layer having a total thickness greater than a height of the dummy gate, polishing the at least one contact metal layer stopping at the dummy gate, and replacing the dummy gate by at least one final gate separated from the substrate by a gate insulating layer, and electrically insulated from the source and drain. Further, depositing the at least one contact metal layer includes depositing a first metal layer and, above the first metal layer, a second metal layer having a greater mechanical resistance to polishing than the first metal layer. In addition, a thickness of the first metal layer is less than the height of the dummy gate, and a total thickness of the first and second layers is greater than the height of the dummy gate. Further, the first metal is chosen from among tungsten and titanium, and the second metal is chosen from among TaN, Ta and TiN.--